

Because the cited references do not separately or in combination teach or suggest these features, the Applicants respectfully submit that claim 1 patently defines the invention over the cited references and should be allowed.

Claim 1 describes a method of synchronizing the operation of *parallel* texture pipelines – that is, synchronizing the operations of *more than one texture pipeline* – by loading each of their state variable queues with polygon state variables, but then only enabling those state variable queues corresponding to the number of parallel texture operations indicated by the state variables. Respectfully, the Examiner has identified no reference or combination that teaches or suggests these features.

Migdal does not describe parallel texture pipelines at all. Instead, *Migdal* describes a method of using a fine grain multi-pass technique to enhance the performance of a single texture pipeline. See, e.g., Abstract; Figs. 1-3, 5; and col. 4:59-61 (“**Only one texture processing hardware unit is used.** Multiple dedicated texture processing hardware units are not necessary.”) (emphasis added).

Possibly recognizing *Migdal*’s failings, the Examiner asserts that *Duluk* provides this missing feature because *Duluk* indicates that, “[a]s a high-performance alternative, multiple pipelines are run in parallel.” See col. 17:14-15. However, *Duluk*’s statement indicates no more than a suggestion to place multiple pipelines side by side and run them at the same time. *Duluk* says nothing about synchronizing parallel pipelines. In fact, neither *Migdal* nor *Duluk* provide any teaching or suggestion concerning any mechanism by which parallel texture pipelines may be coordinated or synchronized. In particular, neither *Migdal* nor *Duluk* describe any means by which all parallel pipelines may be loaded with the same state variables, but only one of the parallel texture pipelines may be subsequently enabled when the state variables indicate that only one parallel texture operation should be performed, as taught by claim 1 of the present invention.

It appears that the Examiner may have confused the concept of multiple sections of a single pipeline with the concept of multiple parallel pipelines. For example, when examining claim 1, the Examiner asserted that “while claim [1] recites synchronizing pipelines, which represents a sequence of processes, it is clear that in Fig. 5 [of *Migdal*], there are four textures are processed in separated sequences depending on the texture number and values received. Therefore, each texture process can be considered as a pipeline that is synchronized by the texture number and

values.” Paper No. 6 at p. 2, ¶ 3. However, while a section of a pipeline may itself be considered a pipeline, it is not true that the various sections of a single pipeline are parallel. Instead, they are linear. Claim 1 recites synchronizing parallel pipelines. No reference cited by the examiner teaches or suggests synchronizing parallel texture pipelines in the manner claimed. Thus, claim 1 is patentable and should be allowed. Similarly, because the remaining claims all recite similar subject matter, they are also patentable and should be allowed for the same reasons as claim 1.

Conclusion

In view of the above amendments and remarks, the Applicants respectfully submit that the present application is now in condition for allowance. A timely Notice to that effect is earnestly solicited. The Examiner is invited to contact the undersigned at (202) 220-4200 to discuss any aspect of the application.

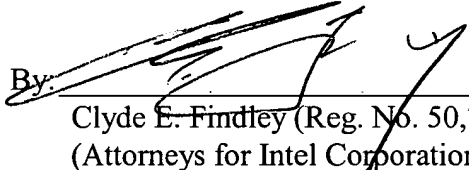
Respectfully submitted,

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Date:

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